adjusted by selecting a mask-defined horizontal dimension. The ability to tailor an ESD protection device's operational threshold voltages such as trigger voltage and holding voltage through selection of horizontal dimensions in the doping masks allows doping dosages to be optimized for other transistors that are simultaneously fabricated, while still minimizing masking steps by simultaneous doping of both types of transistors.

[0064] According to one embodiment, the ESD protection device is connected such that the collector **270** is connected to the terminal **18** of the integrated circuit **5** that is to be protected, and the emitter is connected to the ground supply rail. The base terminal can be left floating or can be connected to the emitter via a resistor. Where a resistor is provided, the voltage difference across the resistor that arises when current flow in the base region has been initiated by impact ionization can be used to further control the "snap back" characteristic of the ESD protection device. This is further discussed below.

[0065] The arrangement described hitherto is suitable for providing unidirectional ESD protection. However, ESD events may occur with either polarity, and hence the integrated circuit benefits from protection against input terminal voltages that are either excessively above its positive supply rail, or excessively below its negative supply rail. In order to achieve this bi-directional ESD protection, two devices can be provided in series.

[0066] Two devices similar to that shown in FIG. **5** are illustrated in FIG. **9**, according to one embodiment. The same numbering is used as in FIG. **5** to refer to like parts, except that the designations "a" and "b" are used as suffixes. Both are horizontal NPN transistors.

[0067] The base regions **120***a* and **120***b* are now drawn as a ring surrounding the emitter regions **130***a* and **130***b*, which serve to delineate the edges of the regions in a slightly different way than was done in FIG. **5**, for purposes of illustrating how the principles and advantages described herein can be obtained using a variety of transistor configurations. The masking and implantation steps remain the same.

[0068] However, intrinsic (high impedance) regions **360***a* and **360***b* have been fabricated just below the emitter regions **130***a* and **130***b* and above the P^+ regions **260***a* and **260***b*. These regions represent additional measures to stop the formation of parasitic components, such as thyristors, that could cause the device to latch into a conducting state.

[0069] In this arrangement the collectors **270***a* and **270***b* are connected together, and the emitter **130***a* and base **120***a* of one of the ESD protection devices is connected to the terminal **18** that is to be protected. The emitter **130***b* and base **120***b* of the other device has a current flow path to a supply rail, and is preferably connected to ground. Thus, for any polarity one of the ESD devices acts as a forward biased diode while the other acts as a reverse biased transistor, and hence breaks down to give the ESD protection when it reaches its trigger voltage. If the polarity of the ESD threat reverses, then the roles of the ESD protection devices reverse, with the one that had previously been acting as a forward biased diode becoming the reverse biased transistor, and the one that had been acting as the reverse biased transistor becoming the forward biased diode. This enables laterally (horizontally) fabricated NPN transistors to provide ESD protection for discharge events of either polarity. The trigger and holding voltages are still defined by the separation between the collector and the base regions, and the size of the base region, respectively within each device. This means the trigger voltages can be set independently for each polarity of ESD threat if desired.

[0070] In other embodiments, other modifications may be made to the ESD protection devices. For example a metal plate **370***b* may be connected to the base or emitter junctions and arranged to extend over the edge of the collector region. This acts as a field plate **370***b* and helps prevent charge injection occurring in the oxide layer over the base-collector junction. Such a field plate **370***b* encircles the emitter when viewed in plan view.

[0071] As noted earlier, the inclusion of a resistor between the base and emitter terminals can modify the turn on characteristic of the device. FIG. **10** illustrates the collector current versus collector voltage characteristics for a device in a grounded emitter configuration, according to two embodiments. Both devices have the same trigger voltage of 40 V, but once the device has triggered, the device with a floating base snaps back more deeply than a similar device with a 6 KΩ, resistor connecting the base and emitter terminals. Thus the resistor helps determine the collector current to turn the horizontal bipolar transistor on.

[0072] Embodiments have been described in the context of NPN devices. PNP structures can also be formed by reversing the dopant conductivity types in the examples provided above. However, carrier mobility is lower in PNP transistors, so they may provide a slower response.

[0073] So far, the structures controlling the breakdown and holding voltages have been described with respect to the devices where these structures are formed at the surface of the device. However, the principles and advantages described herein are not limited to such surface devices. FIG. **11** shows an arrangement where a subsurface or buried NPN bipolar junction determines the trigger voltage, according to one embodiment. In this arrangement, a silicon substrate **400** is provided into which an N-type layer **405** is formed so as to isolate the device from the substrate **400**. An N+ collector **410** is implanted above the layer **405** and, in the finished device, connects to a collector electrode **415** via a vertically extending N-type region **412**. A heavily doped P^+ region **420** is also provided above the N-type layer **405**, and at least part of the region **420** is horizontally aligned with the regions **410**. A P-type region **422** is formed above the P^+ region **420** and makes contact with a base electrode **425**. An N-type region **430** that forms the emitter is deposited within the P-type region **422** and makes connection with an emitter electrode **432**. A resistor **435** may optionally interconnect the base and emitter regions **420** and **430**. The horizontal spacing **450** between the regions **420** and **410** is defined during the masking steps and controls the trigger voltage of the device. The horizontal distance **460** between the emitter **430** and the edge of the P-type base region **422** controls the holding voltage of the device. Thus, both of these parameters are still defined by features which the device designers could "draw," or control by mask design, although not all of these features are coplanar.

[0074] FIG. **12** shows a further embodiment, which is similar to that shown in FIG. **11**, except the horizontal NPN bipolar transistor is now isolated from the rest of the substrate by dielectric isolation comprising a silicon oxide insulating layer **440** at the base of the transistor and trench isolation **455** provided around the sides of the transistor. The choice between electrical junction isolation and dielectric isolation does not have any effect on the operation of the devices described herein. Although reference has been made to form-